1. (Twice Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, said second surface of said semiconductor die being secured to said paddle; and said generally centrally positioned paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars.

2. (Amended) The assembly of claim 1, further comprising:

a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof; and

at least one second connector connected to the at least one connection pad on the lower surface of the first carrier and the at least one circuit on the upper surface of the substrate.

3. The semiconductor device assembly of claim 1, wherein said at least one projection comprises at least one ball deposited by a wire bonding machine.

4. (Amended) The assembly of claim 1, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, at least one first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device; and

encapsulant material filling a portion of the cavity in the first carrier.

5. (Amended) The semiconductor device assembly of claim 1, further comprising:

an electrically non-conductive adhesive layer securing said second surface to said generally centrally positioned paddle.

6. (Amended) An assembly comprising:

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and at least one circuit located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in the at least one aperture in the carrier.

7. (Amended) The semiconductor device assembly of claim 1, further comprising:

an electrically conductive adhesive layer securing said second surface of said semiconductor die to said generally centrally positioned paddle.

8. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a eutectic material.

9. (Amended) The assembly of claim 6, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and at least one circuit located in a portion of the cavity connected to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

10. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

11. (Amended) A semiconductor device assembly comprising:

a first carrier having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, a first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device; and

encapsulant material filling a portion of the cavity in the first carrier.

12. (Amended) The semiconductor device assembly of claim 11, further comprising:

a substrate having an upper surface, a lower surface, and the at least one second circuit on the upper surface thereof; and

at least one second connector connected to the at least one connection pad on the lower surface of the first carrier and the at least one second circuit on the upper surface of the substrate.

13. The semiconductor device of claim 12, further comprising:

sealant packaging material enclosing a portion of said semiconductor die and covering a portion of said substrate.

14. (Twice Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface;

at least one projection secured to said at least one bond pad on said active surface of said semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a metal paddle from a lead frame, said second surface of said semiconductor die being attached to said metal paddle; and said metal paddle is attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

15. The semiconductor device assembly of claim 14, wherein said at least one projection comprises a ball grid array (BGA) of solder balls.

16. (Amended) A semiconductor device assembly comprising:

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and at least one circuit located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in the at least one aperture in the carrier.

17. (Amended) The semiconductor assembly of claim 16, further comprising:

a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof; and

at least one second connector connected to the connector material in the at least one aperture in the carrier and the at least one circuit on the upper surface of the substrate.

18. The semiconductor device assembly of claim 14, further comprising:

an electrically non-conductive adhesive layer attaching said second surface to said paddle.

19. (Amended) The semiconductor device assembly of claim 16, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and at least one circuit located in a portion of the cavity connected to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

20. (Amended) The semiconductor device assembly of claim 14, further comprising:
an electrically conductive adhesive layer attaching said second surface to said metal paddle.

21. (Amended) An assembly comprising:
a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof,
a first carrier having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, at least one first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;
a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;
a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;
encapsulant material filling a portion of the cavity in the first carrier; and
at least one second connector connected to the at least one connection pad on the lower surface of the first carrier and the at least one first circuit on the upper surface of the substrate.

22. The semiconductor device of claim 20, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

23. (Amended) The assembly of claim 21, further comprising:
a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, a first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a

portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device; and

encapsulant material filling a portion of the cavity in the first carrier.

24. The semiconductor device assembly of claim 21, wherein said electrically conductive layer comprises conductive polyimide.

25. (Amended) An assembly comprising:

a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and at least one circuit located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier;

connector material located in the at least one aperture in the carrier; and

at least one second connector connected to the connector material in the at least one aperture in the carrier and the at least one circuit on the upper surface of the substrate.

26. The semiconductor device assembly of claim 25, further comprising:

sealant packaging covering a portion of said semiconductor die and a portion of said substrate.

27. (Twice Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

a plurality of projections connected to said plurality of bond pads for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

28. The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a ball grid array (BGA) of solder balls.

29. (Amended) A semiconductor device assembly comprising:

a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, at least one first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

at least one second connector connected to the at least one connection pad on the lower surface of the first carrier and the at least one first circuit on the upper surface of the substrate.

30. The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a plurality of stud bumps deposited by a wire bonding machine.

31. (Amended) The semiconductor device assembly of claim 29, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, a first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device; and

encapsulant material filling a portion of the cavity in the first carrier.

32. The semiconductor device assembly of claim 31, wherein said adhesive layer comprises one of epoxy and polyimide.

33. (Amended) A semiconductor device assembly comprising:

a substrate having an upper surface, a lower surface, and at least one first circuit on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one aperture extending therethrough, and at least one second circuit located in a portion of the cavity extending to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier;

connector material located in the at least one aperture in the carrier; and

at least one second connector connected to the connector material in the at least one aperture in the carrier and the at least one first circuit on the upper surface of the substrate.

34. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a eutectic material.

35. (Amended) The semiconductor device assembly of claim 33, further comprising:

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and at least one circuit located in a portion of the cavity connected to the at least one aperture;

a semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the second carrier;

a first connector between the at least one circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier; and

connector material located in a second aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

36. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

37. (Amended) An assembly comprising:

a substrate having an upper surface, a lower surface, and at least one circuit on the upper surface thereof;

a first carrier having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, at least one first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a first semiconductor device having an active surface having at least one bond pad thereon, the first semiconductor device located within the cavity of the first carrier;

a first connector between the at least one second circuit located in a portion of the cavity of the first carrier and the at least one bond pad on the active surface of the first semiconductor device;

encapsulant material filling a portion of the cavity in the first carrier;

at least one second connector connected to the at least one connection pad on the lower surface of the first carrier and the at least one first circuit on the upper surface of the substrate;

a second carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, at least one first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a second semiconductor device having an active surface having at least one bond pad thereon, the second semiconductor device located within the cavity of the second carrier;

a second connector between the at least one second circuit located in a portion of the cavity of the second carrier and the at least one bond pad on the active surface of the second semiconductor device;

encapsulant material filling a portion of the cavity in the second carrier;

at least one third connector connected to the at least one connection pad on the lower surface of the second carrier and the at least one first circuit on the lower surface of the substrate.

38. The semiconductor device of claim 27, further comprising:

a substrate having a plurality of circuit connections, said plurality of bond pads connected to said plurality of circuit connections.

39. (Amended) The assembly of claim 37, further comprising:

a third carrier oriented with respect to the first carrier and positioned the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, at least one connection pad on the upper surface, at least one connection pad on the lower surface, a first circuit connecting the at least one connection pad on the upper surface to the at least one connection pad on the lower surface, and at least one second circuit located in a portion of the cavity connected to one of the at least one connection pad on the upper surface and the at least one connection pad on the lower surface;

a third semiconductor device having an active surface having at least one bond pad thereon, the semiconductor device located within the cavity of the third carrier;

a fourth connector between the at least one first circuit located in a portion of the cavity of the third carrier and the at least one bond pad on the active surface of the semiconductor device; and

encapsulant material filling a portion of the cavity in the third carrier.